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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,977	06/19/2005	Willem A Sloof	US 020632	8347

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EXAMINER	
RAINEY, ROBERT R	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/539,977	SLOOF ET AL.	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6-19-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Examiner particularly encourages the addition of headings (f) to (j).

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in

compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,384,817 to *Janssen et al.* ("*Janssen*") ") in view of U.S. Patent No. 5,166,671 to *Maekawa* ("*Maekawa*") and further in view of U.S. Patent No. 5,568,062 to *Kaplinsky* ("*Kaplinsky*").

As to **claims 1, 7-10, and 14-17**, *Janssen* discloses a liquid crystal display device and in particular:

A video driver for display device, comprising: a buffer amplifier adapted to receive and buffer a voltage ramp input signal, the buffer amplifier comprising, an input stage adapted to receive the voltage ramp input signal, and an output stage adapted to provide a video output signal (see for example Fig. 2 items 22 and

30), and a feedback path between the output stage and the input stage adapted to cause the video output signal to follow the voltage ramp input signal when the output stage is enabled (see for example Fig. 2 feedback path for item 30).

Janssen does not expressly disclose an output stage comprising a pair of output stage transistors connected in series between a first supply voltage and a second supply voltage; and a first sample-and-hold switch arranged between a control terminal of a first one of the output stage transistors and the first supply voltage, the first sample-and-hold switch being responsive to a first sample-and-hold control signal to selectively connect the control terminal of the first one of the output stage transistors to the first supply voltage and turn off the first one of the output stage transistors; and a second sample-and-hold switch arranged between a control terminal of a second one of the output stage transistors and the second supply voltage, the second sample-and-hold switch being responsive to a second sample-and-hold control signal to selectively connect the control terminal of the second one of the output stage transistors to the second supply voltage and turn off the second one of the output stage transistors.

Maekawa discloses a liquid crystal display device and in particular: an output stage comprising a pair of output stage transistors connected in series between a first supply voltage and a second supply voltage (see for example Fig. 5 items N_3 and P_5) and first and second sample-and-hold control signals (see for example Fig. 3 items ϕ_{H1} and its complement); and charging a capacitor (see for example Fig. 3 item C_{11}).

Janssen and *Maekawa* are analogous art because they are from the same field of endeavor, which is liquid crystal displays.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to use the buffer amplifier as disclosed by *Maekawa* as the buffer amplifier of undisclosed particulars in the device after *Janssen*. The suggestion/motivation would have been to utilize a known design choice.

Janssen and *Maekawa* disclose the claimed invention except for a first sample-and-hold switch arranged between a control terminal of a first one of the output stage transistors and the first supply voltage, the first sample-and-hold switch being responsive to a first sample-and-hold control signal to selectively connect the control terminal of the first one of the output stage transistors to the first supply voltage and turn off the first one of the output stage transistors; and a second sample-and-hold switch arranged between a control terminal of a second one of the output stage transistors and the second supply voltage, the second sample-and-hold switch being responsive to a second sample-and-hold control signal to selectively connect the control terminal of the second one of the output stage transistors to the second supply voltage and turn off the second one of the output stage transistors.

Kaplinsky discloses a buffer circuit and in particular: a first switch (see for example Fig. 1 item 31) arranged between a control terminal of a first one of the output stage transistors (see for example Fig. 1 item 11) and the first supply voltage, the first switch being responsive to a first control signal (see for example

Fig. 1 item OE) to selectively connect the control terminal of the first one of the output stage transistors to the first supply voltage and turn off the first one of the output stage transistors (see for example column 3 lines 29-35); and a second switch (see for example Fig. 1 item 37) arranged between a control terminal of a second one of the output stage transistors (see for example Fig. 1 item 17) and the second supply voltage, the second switch being responsive to a second control signal (see for example Fig. 1 item S2) to selectively connect the control terminal of the second one of the output stage transistors to the second supply voltage and turn off the second one of the output stage transistors (see for example column 3 lines 29-35).

The prior art device of *Kaplinsky* comprises a digital buffer improved with the capability, as described above, to shut down the output drive transistors in order to prevent circuitry connected to the output from drawing current from or sourcing current into the output of the buffer. This is commonly referred to as a tri-state buffer. One of ordinary skill in the art at the time of the invention could have applied the known output drive shutdown technique in the same way to the buffer after *Maekawa* and the results would have been predictable to one of ordinary skill in the art.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to provide shutdown capability for the output drive transistors of *Maekawa* after the manner suggested by *Kaplinsky*. The

suggestion/motivation would have been to prevent unnecessary current dissipation when the buffer is idle or to perform the tri-state function.

As to **claim 2**, in addition to the rejection of claim 1 over *Janssen*, *Maekawa* and *Kaplinsky*, *Kaplinsky* further discloses that the first and second sample-and-hold switches each comprise a transistor (ibid.).

As to **claim 3**, in addition to the rejection of claim 1 over *Janssen*, *Maekawa* and *Kaplinsky*, *Kaplinsky* further discloses a pair of sample-and-hold control terminals connected to control terminals of the first and second sample-and-hold switches and providing thereto the first and second sample-and-hold control signals (see for example Fig. 1).

As to **claims 4, 11 and 18**, in addition to the rejection of claim 1 over *Janssen*, *Maekawa* and *Kaplinsky*: *Maekawa* further discloses a transmission gate between the buffer and a driven circuit (see for example Fig. 1 item M_{b1}).

Janssen, *Maekawa* and *Kaplinsky* disclose the claimed invention except for a transmission gate in the feedback path between the output stage and the input stage. It would have been obvious to one having ordinary skill in the art at the time the invention was made to move the transmission gate from the position shown in *Maekawa* to a position in the feedback path, since it has been held that rearranging parts of an invention involves only routine skill in the art, In re

Japikse, 86 USPQ 70. In both instances the transmission gate performs the same function; it isolates the driven from the driving circuit.

As to **claim 5, 12 and 19**, in addition to the rejection of claim 4 over *Janssen*, *Maekawa* and *Kaplinsky*: *Maekawa* further discloses that the transmission gate comprises a complementary pair of transistors (ibid.).

As to **claim 6, 13 and 20**, in addition to the rejection of claim 5 over *Janssen*, *Maekawa* and *Kaplinsky*: *Maekawa* further discloses a pair of sample-and-hold control terminals connected to control terminals of the complementary pair of transistors of the transmission gate (ibid.).

Claim Objections

2. Claim 16 objected to because of the following informalities: "wherein the wherein the" is not a standard construction. Appropriate correction is required.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER

/RR/